Amendments to the Specification

Please add the following new heading and paragraph after the title at page 2, line 1, and before the heading BACKGROUND OF THE INVENTION at page 2, line 3:

CROSS-REFERENCE TO PRIOR APPLICATIONS

This application is a continuation of U.S. Patent Application number 09/276,474, filed March 25, 1999, which is a continuation of U.S. Patent Application 08/814,042, filed on March 10, 1997, now U.S. Patent number 5,991,898, issued November 23, 1999, both of which are hereby incorporated by reference.

Please replace the paragraph beginning at page 14, line 24, with the following amended paragraph:

In other words, in accordance with the present invention, exemplary IC 10 is provided with ABIST through microcode that leverage on the mission logic of embedded processor core 12, requiring only one extra register in terms of hardware, i.e. test port register 20. Thus, there are virtually no area requirement, nor performance impact on exemplary IC 10. Before further describing how ABIST is provided to exemplary IC 10, it should be noted that why the present invention is being described with the exemplary IC 10 having non-volatile memory 18 storing the various microcode implementing the arithmetic pseudo-random test vector generator, arithmetic parallel decompressor, and arithmetic test response compactors, and so forth, the

present invention may be practiced with some or all of the microcode stored in non-volatile or volatile storage medium disposed inside or outside the IC.

Please replace the paragraph beginning at page 18, line 15, with the following amended paragraph:

The ability to produce any q-tuple, regardless of location of bits of interest, is the next quality criteria considered. In contrast to LFSR-based generators, the arithmetic pseudo-random test vector generator of the present invention features non-linear dependencies originating from the congruential multiplicative formula used. These dependencies have been examined by Monte Carlo simulations with the objective of determining the probability that randomly selected q positions of the output sequence cannot be covered by some combinations of 0s and 1s, i.e., given a sequence of generated bits, it is verified whether the sequence contains q-bit pattern of 0s and 1s which matches a pre-computed vector of binary values and distances between positions on which these values occur. The Monte Carlo simulations have also been used to analyze corresponding dependencies in LFSR-generated sequence, as the existing closed-form solution of the linear dependency problem cannot be used for sequences shorted than 2.sup.n -1, as was shown by J. Rajski and J. Tyszer in the paper entitled "On Linear Dependencies in Subspaces of LFSR-Generated Sequences,", IEEE Transactions on Computers, ~~<vol & date info, to be inserted>~~ Vol. 45, No. 10, October 1996.

Please replace the paragraph beginning at page 26, line 23, with the following amended paragraph:

Experiments were performed on the largest ISCAS'89 circuits described by F. Brglez, D. Bryan, and K. Kozminski in the paper entitled "Combinational Profiles of Sequential Benchmark Circuits". Proc. Int Symp. on Circuits and Systems, 1989, pp. 1929-1934, assuming a data path of width 8, 16, or 32. Furthermore, the number of scan chains was assumed to be equal to the width of the data path. For a width n, a single length L is chosen for each of n LFSR-based segments for a given circuit, where L is greater than n as well as greater than s+20, where s is the maximum number of specified bits in a test vector. Recall that this requirement insures that a seed can be obtained with probability greater than 0.999999. The LFSR-based segments were linked together by an XOR interconnection network such that the network connects the ith segment to segment number i+2.sup.v (mod n), for v=0, 1, . . . , log.sub.2 n-1. Note that the polynomial used to implement the decompressor should contain a sufficient number of feedback taps in order the reduce the probability of linear dependency, as was ~~suggest~~ suggested by J. Rajski and J. Tyszer in the paper entitled "On Linear Dependencies in Subspaces of LFSR-Generated Sequences,", IEEE Transactions on Computers, ~~<vol & date info, to be inserted>~~ Vol. 45, No. 10, October 1996. Consequently, the probability of not finding a seed for a given test pattern will be minimized as well. In order to minimize the number of instructions executed per cycle, inter-segment connections were simplified whenever possible.

Please delete the paragraph beginning at page 48, line 3, which starts with "In one embodiment, an IC with an embedded processor core. . ."

Please add the following new paragraph at page 48, line 3:

An apparatus and method provide for an arithmetic built-in self test (ABIST) of a number of peripheral devices having parallel scan registers coupled to a processor core, all within an integrated circuit. Using the data paths of the processor core, operating logic generates pseudo-random test patterns for the peripheral devices, employing a mixed congruential generation scheme. In one embodiment, generating the pseudo-random test patterns includes multiplying n least significant bits of a 2n-bit pseudo-random number generated in an immediately preceding iteration and stored in a first register, with an n-bit multiplier constant stored in a second register to produce a 2n-bit product, adding the 2n-bit product to n most significant bits of the 2n-bit pseudo-random number stored in n least significant locations of an accumulator with 2n locations to produce a new 2n-bit pseudo-random number for a current iteration, and outputting n least significant bits of the new 2n-bit pseudo-random number as an n-bit pseudo-random test vector for the peripheral devices.